SHRI VENKATESHWARA UNIVERSITY

Syllabus

M.TECH (VLSI) PART TIME

(Two Years Post Graduation Programme)

II SEMESTER
(w.e.f. 2019-20)

SCHOOL OF ENGINEERING & TECHNOLOGY

SEMESTER-II													
Sl. No.	**Subject Codes**	**Subject**	**Periods**			**Evaluation Scheme**				**End Semester**		Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	WVI-201	Analog and Digital CMOS VLSI Design	3	0	0	20	10	30		70		100	3
2	WVI-023	Low power VLSI Design	3	0	0	20	10	30		70		100	3
3	WVI-211	Analog and Digital CMOS VLSI Design Lab	0	0	4				25		25	50	2
4	AUD-102	Disaster Management	0	0	0	20	10	30		70		100	0
		Total										350	8

Code	Course Name	L-T-P	Cr.
WVI-201	Analog and Digital CMOS VLSI Design	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Syllabus Contents:

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process

Digital CMOS Design:

Unit 1: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout,Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noisemargin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3: Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

Unit 4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common- gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbertcell.

Unit 5: Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise.

Unit 6: Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

References:

- J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
- BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
- R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
- Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Code	Course Name	L-T-P	Cr.
WVI-211	Analog and Digital CMOS VLSI Design Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Processand VDD=1V for 0.09um CMOS Process.

a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS =30mV.

To extract Vth use the following procedure.

I. Plot gm vs VGS using NGSPICE and obtain peak gm point.

II. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.

III. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.

f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC loadline and calculate gm, gds, gm/gds, and unity gain frequency.

Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Processand VDD=1V for 0.09um CMOS Process.

a) Perform the following

I. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.

II. Plot VTC for CMOS inverter with varying VDD.

III. Plot VTC for CMOS inverter with varying device ratio.

b) b) Perform transient analysis of CMOS inverter with no load and with loadand determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF).

c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)

3) 3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

I. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

II. Calculate input bias voltage if bias current=50uA.

III. Use Ngspice and obtain the bias current. Compare its value with 50uA.

IV. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

V. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constantresulted from -3dB BW

VI. Use Ngspice to determine input voltage range of the amplifier

5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

I. Draw the schematic of op-amp macro model.

II. Draw the schematic of INA.

III. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain = 5x104,
b. unity gain BW (fu) = 500KHz,
c. input capacitance=0.2pF,
d. output resistance = ,

e. CMRR=120dB

IV. Draw schematic diagram of CMRR simulation setup.

V. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

VI. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explainhow CMRR of OPAMP changes with resistor mismatches.

VII. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimumsized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.

d) Use interconnect length obtained and connect the second and third inverter. Extract the new netlist and obtain tPHL and tPLH of the middleinverter. Compare new values of delay times with corresponding valuesobtained in part 'c'.

Code	Course Name	L-T-P	Cr.
WVI-023	Low power VLSI Design	3-0-0	3

Course Outcomes: At the end of the course, students will be able to:

- CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- CO2: Characterize and model power consumption & understand the basic analysis methods.
- CO3: Understand leakage sources and reduction techniques.

Syllabus Contents:

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches,dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction,transistor sizing & optimal gate oxide thickness, impact of technology scaling,technology innovations.
Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver

versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6: Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

References:

- P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wileysons Inc.,2000.
- J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, 1995.
- Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.